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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,342	09/26/2003	Hirotomo Ishii	243324US2S	5069

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EXAMINER	
PATEL, DHARTI HARIDAS	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 05/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/670,342	ISHII, HIROTOMO	
	Examiner	Art Unit	
	Dharti H. Patel	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6, 8-25* is/are pending in the application.

4a) Of the above claim(s) *8-25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/7/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over the acknowledged prior art, in view of Mizuno et al., Publication No. US2003/0102904A1. With respect to claim 1, applicant's acknowledged prior art [Fig. 7] teaches a semiconductor integrated circuit that comprises a first circuit block [Fig. 7, 104] including a first power supply terminal [Fig. 1, 102] and a first ground terminal [Fig. 7, 103], a first power supply voltage being applied between the first power supply terminal [Fig. 7, 102] and the first ground terminal [Fig. 7, 103] from a first power domain [Fig. 7, 101]; a second circuit block [Fig. 7, 204] including a second power supply terminal [Fig. 7, 202] and a second ground terminal [Fig. 7, 203], a second power supply voltage being applied between the second power supply terminal [Fig. 7, 202] and the second ground terminal [Fig. 7, 203] from a second power domain [Fig. 7, 201], at least one of the second power supply terminal and the second ground terminal being provided independently of one of the first power supply terminal and the first ground terminal; a propagation circuit [Fig. 7, 401] provided between an output terminal of the first circuit block [Fig. 7, 104] and an input terminal of the second circuit

block [Fig. 7, 204] to propagate a signal; and an electrostatic discharge protection circuit [Fig. 7, 601] connected to the first and second power supply terminals [Fig. 7, 102 and 202] and the first and second ground terminals [Fig. 7, 103 and 203, Specification, Page 2, lines 14-21 and Fig. 7]. Applicant's acknowledged prior art [Fig. 10] further teaches that a signal input element [Fig. 10, MP2 or MN2] is connected to the input terminal of the second circuit block [Fig. 10, 204] to which the signal [Fig. 10, 401] is input through the propagation circuit.

However, the prior art fails to teach or suggest a second circuit block that includes a plurality of elements having an equal input withstanding voltage; the first circuit block includes a plurality of elements whose withstanding voltage is equal to or lower than that of the elements of the second circuit block; and a signal input element connected to the input terminal of the second circuit block to which the signal is input through the propagation circuit has an input withstanding voltage which is higher than that of other elements of the second circuit block.

With respect to the limitation of elements having an equal input withstanding voltage in each block, it is well known in the art the components of a second circuit block of any system must be designed to handle equal or less withstanding voltage than the output of the first (cascaded) circuit block, otherwise the components of the second circuit block will be damaged due to excessive voltage outputted from the first circuit block. Additionally, the elements

in each block must themselves have an equal input withstanding voltage, or damage to those elements can occur.

Mizuno et al. teaches a semiconductor integrated circuit device. Mizuno et al. teaches that the signal input element has an input withstanding voltage, which is higher than that of other elements of the circuit block [Page 8, Paragraph 0090, lines 24-28].

Both teachings are related by being semiconductor integrated circuit devices. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was to made to combine the teachings of Mizuno et al., which teaches an input buffer generally having a high withstanding voltage, into the semiconductor device of the applicant's acknowledged prior art because joint use of the transistors in I/O circuit allows a reduction of the type of MOS transistor gate dielectric used in the overall chip and consequently the cost can be reduced.

With respect to claim 2, applicant's acknowledged prior art teaches that the propagation circuit is a signal line [Fig. 7, 401], which makes a short circuit between the output terminal of the first circuit block [Fig. 7, 104] and the input terminal of the second circuit block [Fig. 7, 204, Specification, Page 2, lines 23-26 and Fig. 7].

With respect to claim 3, applicant's acknowledged prior art teaches that the elements of the second circuit block [Fig. 7, 204] are a plurality of MOS transistors [Specification, Page 6, lines 16-18 and Fig. 10].

With respect to claim 5, applicant's acknowledged prior art teaches that the first power supply voltage [Fig. 7, 102] and the second power supply voltage [Fig. 7, 202] are equal to each other [Specification, Page 3, lines 24-26].

With respect to claim 6, applicant's acknowledged prior art teaches that the first power supply voltage [Fig. 7, 102] and the second power supply voltage [Fig. 7, 202] differ from each other [Specification, Page 3, lines 22-23 and Page 4, lines 1-3].

2. With respect to claim 4, applicant's acknowledged prior art [Fig. 10] teaches that the elements of the second circuit block [Fig. 10, 204] are a plurality of MOS transistors but does not disclose that a gate oxide of a MOS transistor that forms a signal input element is thicker than that of another MOS transistor that forms another element.

Mizuno et al. teaches that a gate oxide of a MOS transistor that forms a signal input element is thicker than that of another MOS transistor that forms another element [Page 8, Paragraph 0090, lines 24-28].

Both teachings are related by being semiconductor integrated circuit devices. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was to made to combine the teachings of Mizuno et al., which teaches an input buffer generally having a high withstanding voltage, into the semiconductor device of the applicant's acknowledged prior art because joint use of the transistors in I/O circuit allows a reduction of the type of MOS

transistor gate dielectric used in the overall chip and consequently the cost can be reduced.

Response to Arguments

3. With respect to the arguments on page 11, lines 17-23, applicant's claim language is directed towards "a signal input element connected to the input terminal of the second circuit block to which the signal is input through the propagation circuit has an input withstanding voltage which is higher than that of other elements of the second circuit block;" which is disclosed by applicant's acknowledged prior art in combination with Mizuno. Applicant's prior art teaches a signal input element [Fig. 10, MP2, and MN2] connected to the input terminal of the second circuit block [Fig. 10, 204] to which the signal is input through the propagation circuit [Fig. 10, 401]. Mizuno teaches that a signal input element has an input withstanding voltage, which is higher than that of other elements of the second circuit block [Page 8, paragraph 0090, lines 24-28].

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory

action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dharti H. Patel whose telephone number is 571-272-8659. The examiner can normally be reached on 8:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800, Ext. 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DHP
04/25/2006

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